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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,039	07/14/2003	Yasushi Koubuchi	501.36127CC3	6056

20457 7590 02/01/2007

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/619,039	Applicant(s) KOUBUCHI ET AL.	
	Examiner Long Pham	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 11, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Element isolation insulating films 8,9 completely filling said trenches serving as element isolation regions, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 11, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 11, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 12, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals 17a,17b. See fig. 4 and associated text.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 13, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Insulating films 8,9 completely filling said trenches serving as element isolation regions, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 13, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 13, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 14, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals 17a,17b. See fig. 4 and associated text.

Further with respect to claim 14, Hirabayashi fails to teach forming bonding pads at external terminals.

However, the formation of bonding pads at external terminals to allow interconnection is well-known in semiconductor art.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 15, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Element isolation insulating films 8,9 completely filling said trenches, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 15, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 15, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 16, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals 17a,17b. See fig. 4 and associated text.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 17, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

A trench 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

An element isolation insulating film 8,9 completely filling said trench serving as element isolation regions wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 17, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 17, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 11, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Element isolation insulating films 8,9 completely filling said trenches serving as element isolation regions, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 18, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 18, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 19, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals 17a,17b. See fig. 4 and associated text.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 20, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Insulating films 8,9 completely filling said trenches serving as element isolation regions, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 20, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 20, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 21, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals 17a,17b. See fig. 4 and associated text.

Further with respect to claim 21, Hirabayashi fails to teach forming bonding pads at external terminals.

However, the formation of bonding pads at external terminals to allow interconnection is well-known in semiconductor art.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 22, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

Trenches 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

Element isolation insulating films 8,9 completely filling said trenches, wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 22, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 22, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

With respect to claim 23, Hirabayashi further teaches a length of each of said dummy regions is shorter than a distance between external terminals.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi (US pat 5,614,445) in combination with Ogawa et al. (US pat 4,506,434).

With respect to claim 24, Hirabayshi teaches a semiconductor integrated circuit device comprising (see figs. 1-12 and associated text):

A trench 4,6 formed in a semiconductor substrate 1,2 and defining active regions (where between trenches 4,4 and trenches 6,6) and dummy regions 5 (fig. 6); and

An element isolation insulating film 8,9 completely filling said trench serving as element isolation regions wherein dummy regions are formed at a scribing area with inherently a number, size, and layout, and a surface of said element isolation insulating films filled in said trenches at said scribing area is planarized.

Hirabayashi teaches the isolation trench is completely filled with part insulator material and part polysilicon but fails to teach the isolation trench is completely filled only with insulating material.

Ogawa et al. teach forming a trench isolation in which isolation trench is completely filled with insulator material 47 only to provide better isolation (as compared to thermal oxide) for devices on the substrate 41.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate teaching of Ogawa et al. into the device of Hirabayashi to achieve the above benefit.

Further with respect to claim 24, how the element isolation insulating films are planarized has not been given patentable weight because claims are directed to a structure.

Further with respect to claim 24, how the element isolation insulating films fill the trenches has not been given patentable weight because claims are directed to a structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP